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Description

METHOD FOR REACTIVE ION ETCH PROCESSING OF A DUAL DAMASCENE STRUCTURE

BACKGROUND OF INVENTION

[0001] The present invention relates generally to semiconductor device processing, and, more particularly, to a method for reactive ion etch processing of dual damascene structures formed in porous dielectric materials.

[0002] In the fabrication of integrated circuit devices, it is often desirable to isolate individual components of the integrated circuits from one another with insulative materials. Such insulative materials may include, for example, silicon dioxide, silicon nitride and silicon carbide. While these materials may have acceptable insulating properties in many applications, they also have relatively high dielectric constants, which can lead to capacitive coupling between proximate conductive elements. This is particularly disadvantageous, given the ever-decreasing distances between

conductive circuit elements, and the use of multi-layered structures. An unnecessary capacitive coupling between adjacent wires increases the RC time delay of a signal propagated therethrough, resulting in decreased device performance.

[0003] Thus, for specific applications, insulating materials having relatively low dielectric constants (e.g., $k < 3$) are desired. In very large scale integrated circuit (VLSI) technology, silicon dioxide (SiO_2) has been traditionally used as an inter-level dielectric (ILD) material in conjunction with aluminum interconnect material. More recently, however, significant advancements have been made to enhance circuit performance by replacing the SiO_2 with a "low-k" dielectric and by using copper (higher conductivity) interconnect.

[0004] Organic materials or materials of low density used as low-k dielectrics are frequently etched when the resist is stripped from the wafer. This results in vias being etched too deeply or completely etched to a sub-film before the resist is removed. To overcome this drawback, a dual damascene reactive ion etch (RIE) process is split into two discrete steps where the vias are etched first, followed by the trench definition. The reverse of this process is also

used, wherein the trench pattern is etched prior to the vias. In either case, however, stripping of the resist presents problems of depth and profile control.

[0005] Furthermore, organosilciate (OSG) type materials used as dielectrics are sensitive to wet cleaning steps, such as a dilute hydrofluoric acid (DHF) rinse. For example, a porous OSG film has been shown to etch in DHF solutions. In addition, the absorption of liquid matter in the pores of the dielectric can pose a major problem to the liner integrity. Accordingly, it would be desirable to be able to implement a damage free etch process that isolates the dielectric layer from resist stripping steps, while also controlling etch rate of the dielectric layer and maintaining a robust processing window.

SUMMARY OF INVENTION

[0006] The foregoing discussed drawbacks and deficiencies of the prior art are overcome or alleviated by a method for implementing dual damascene processing. In an exemplary embodiment, the method includes forming a first hardmask layer over an interlevel dielectric layer, and forming a second hardmask layer over the first hardmask layer. A trench pattern is opened within a third hardmask layer formed over the second hardmask. A first etch pro-

cess is implemented so as to define a via pattern completely through the second hardmask layer and partially through the first hardmask layer, and a second etch process is implemented to transfer the trench pattern and the via pattern into the interlevel dielectric layer.

[0007] In another embodiment, a method for implementing dual damascene processing for a semiconductor device includes forming a first hardmask layer over an interlevel dielectric layer and forming a second hardmask layer over the first hardmask layer. A trench pattern is opened within a third hardmask layer formed over the second hardmask. A first etch process is implemented so as to define a via pattern completely through the second hardmask layer and partially through the first hardmask layer. A photoresist layer used to create the via pattern is stripped, and a second etch process is then implemented to transfer the trench pattern and the via pattern into the interlevel dielectric layer.

BRIEF DESCRIPTION OF DRAWINGS

[0008] Referring to the exemplary drawings wherein like elements are numbered alike in the several Figures:

[0009] Figures 1(a) through 1(f) are cross sectional views illustrating a method for implementing dual damascene pro-

cessing, in accordance with an embodiment of the invention.

Detailed Description

[0010] Disclosed herein is a processing scheme in which an organic or low density, low-k dielectric film is provided with additional hardmask layers thereupon, such that the lower hardmask layer is direct contact with the dielectric is only partially etched therethrough during initial via/trench definition. In this manner, a photoresist material may be stripped without exposing the low-k material to the removal process. Thereafter, the remaining lower hardmask layer is removed, and a different etch chemistry is employed for completing the via and trench definition within the dielectric layer, down to a cap layer thereunderneath.

[0011] Referring initially to Figure 1(a), there is shown a cross sectional view of a wafer film stack of a semiconductor device having patterned resist for vias in the trench region of a previously etched tantalum nitride (TaN) hardmask. More particularly, a lower layer 102 (e.g., a substrate or lower level metallization layer) has a cap layer 104 (e.g., silicon nitride, silicon carbide) formed thereon, followed by a dielectric layer 106. The dielectric layer 106 may be an organic, low-k material such as SiLK® or porous OSG,

for example. Then, a first hardmask layer 108 is formed directly over the dielectric layer 106, followed by a second hardmask layer 110 formed over the first hardmask layer 108. In an exemplary embodiment, the first hardmask layer 108 may be a low-k dielectric barrier such as BLOk ™, while the second hardmask may be silicon nitride (SiN), for example.

[0012] In addition, a third hardmask layer 112, such as tantalum nitride (TaN) for example, is formed over the second hardmask layer 110. In Figure 1(a), the TaN hardmask layer 112 is shown opened in accordance with a metal trench pattern defined in accordance with dual damascene processing. A layer of photoresist material 114 is further formed over the TaN hardmask layer 112 and exposed portions of the second hardmask layer 110, after which a pair of via openings 116 are patterned within the photoresist 114.

[0013] As shown in Figure 1(b), a first etch process is used to transfer the via pattern completely through the SiN second hardmask layer 110, and an associated antireflective coating layer (not shown). Once completely through the second hardmask layer 110, the first etch process continues to partially etch through the thickness of the first hard-

mask layer 108. In an exemplary embodiment, the first etch process etches through at least about 50% of the thickness of the first hardmask layer 108, and more preferably through at least about 60% of the thickness. In order to control the partial etching of the first hardmask layer, the etch chemistry of the first etch process is preferably selected such that the second hardmask layer 110 etches at a faster rate than the first hardmask layer 108.

[0014] Once the desired amount of the first hardmask layer 108 is removed, the photoresist layer 114 is stripped as shown in Figure 1(c), and the wafer may be wet-cleaned with a DHF rinse, for example. Because there is still a remaining thickness of the first hardmask layer 108, the dielectric layer 106 underneath is not subjected to the stripping/ rinse chemistry. Thus, a dielectric material having a high etch rate in DHF, such as porous OSG (p-OSG), is undamaged as a result of the resist stripping and cleaning environment.

[0015] Then, as shown in Figure 1(d), a second etch process is commenced so as to transfer both the predefined trench and via patterns into the dielectric layer 106. The chemistry and plasma conditions of the second etch process

are (different etch rate/different gasses not selective to blok, but faster). During this etch, the newly exposed (and previously unetched portions) of the second and first hardmask layers begin to be removed (i.e., the trench hardmask open process). However, before those portions are completely removed, the via pattern will first clear through the previously thinned portions of first hardmask layer 108. Once this occurs, the via pattern will then accelerate into the dielectric layer 106, due to its faster etch rate. By the time the second and first hardmask layers 110, 108 exposed by the trench pattern are completely removed, the vias 116 formed in dielectric layer 106 are already about 60% or more through the total thickness thereof.

[0016] Accordingly, when the trench pattern reaches the dielectric, the etch rate thereof will be the same as the increased etch rate of the via 116. The second etch process is completed once the cap layer 104 is reached, as shown in Figure 1(e). The accelerated etch rate of the trench pattern into the dielectric material for the remaining time taken for the via depth to reach the cap layer 104 results in a desired trench depth of about 35% to about 40% of the overall thickness of the dielectric layer 106. Finally, in

Figure 1(f), the cap layer 104 is etched to allow electrical connection to the lower level layer 102. Another DF cleaning step can be performed in a non-damaging environment, such as Ar/H_2, before the trench and vias are filled with conductive materials and thereafter planarized in accordance with established damascene processing techniques.

[0017] As will be appreciated, the above described approach to defining dual damascene trench and via patterns within a porous, low-k dielectric (or OSG) material is advantageous in that a non-damaging resist removal process may be implemented within an integrated, single chamber RIE processing tool. In other words, the techniques described herein provide a significant cost advantage over existing non-damaging resist removal processes (or, alternatively damage recovery processes) such as applying an He/H_2 downstream plasma in a separate plasma processing tool, silation, and annealing for example.

[0018] While the invention has been described with reference to a preferred embodiment or embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention.

In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.

[0019] WHAT IS CLAIMED IS: